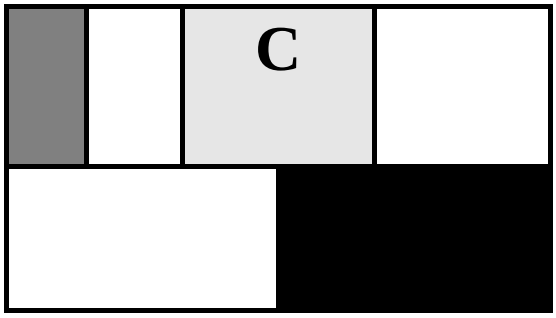
ADDENDUM



NON-SILICON DIGITAL CIRCUITS

Designing high speed logic in GaAs

n

Extreme performance using cryogenic techniques

C.1 Introduction

This chapter deals with the design of digital integrated circuits with operating speeds in the multiple hundreds of MHz, and even the GHz range. These speeds are desirable in the core processors of super- and mainframe computers, and even high-end workstations. High performance is also a prime requirement in the domain of high-speed signal-acquisition apparatus, such as digital sampling oscilloscopes. Measurement equipment must always be faster than the circuits it observes; hence the need for high-speed logic. With the advent of optical fiber, digital communication systems have been extended into the Gbits/sec area and need extremely high-speed front-end circuitry. Finally, the availability of high-speed technologies simplifies the task of automating the design process for high-performance circuits.

In our quest for these ever higher speeds, even bipolar designs eventually reach a maximum. When extreme performance is a necessity, room-temperature silicon is replaced by other semiconductor materials such as gallium arsenide (GaAs). The lure of GaAs and other compound semiconductors is a substantial increase in carrier mobility and, hence, performance. An alternative solution is to opt for operation at a reduced temperature. Lowering the temperature reduces the delay of traditional semiconductor components. Some materials even have the property of becoming superconductive when operated below a certain temperature, which eliminates resistivity altogether. Circuits with mind-boggling performance can be conceived using these technologies.

C.2 Digital Gallium Arsenide Design

The combination of the latest manufacturing technology and advanced circuit design makes it possible to realize inverters with propagation delays of around 20 psec in silicon bipolar. Once again, treat this value with caution, as it is obtained in an ideal structure such as a ring oscillator (with a fan-out of 1). The actual gate delay that can be achieved in actual designs is at least twice as large, and more often many times higher. When faster switching speeds are required such as in the next generation of super-computers or in the front-end of advanced radio-telecommunication devices, silicon-based designs run out of steam.

This does not mean that going faster is out of the question. Other semiconductor materials, such as gallium arsenide (GaAs) and silicon-germanium (SiGe), have switching properties that exceed the performance of silicon. In the next sections, some attention is devoted to the design of digital gates in these technologies. Although these approaches represent only a small fraction of the digital design market, it is valuable to have an impression of how digital design for very high speed is conducted. We will limit ourselves to a discussion of GaAS-based design.

C.2.1 GaAs Devices and Their Properties

GaAs Material Properties

The performance of submicron silicon MOS devices is constrained by the maximum electron-drift velocity υ_{sat}, which approximately equals 10^7 cm/sec. As this is an intrinsic property of the material, faster switching speeds can only be achieved by a scaling of the technology or by exploring other semiconductor materials. An example of the latter is gallium-arsenide, which is a compound semiconductor material that has the intrinsic capability of being approximately twice as fast as silicon. Figure C.1 plots the carrier velocity of

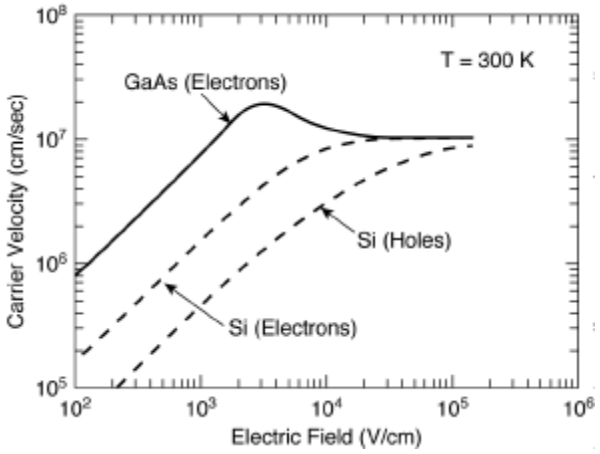


Figure C.1 Measured carrier velocity versus electric field for Si and GaAs [Sze69].

electrons and holes in both GaAs and Si as a function of the electrical field. For lower field strengths, the velocity is proportional to the field for all carriers. For higher field values, the carrier velocity saturates to approximately 10^7 cm/sec, independent of the material or the carrier. The most important lesson to be learned from this graph is that at lower values of the electrical field, GaAs electrons display a higher velocity, peaking at 2×10^7 cm/sec before dropping to the saturation value. The velocity increase is due to the lower *effective mass* m_e of the GaAs electrons compared to Si. When operated at low electrical fields, GaAs has the capability of being substantially faster than Si. A number of the important properties of GaAs are enumerated below.

- When operated at low electrical fields, *n*-type GaAs circuits can be *twice as fast as silicon circuits*. To exploit this feature requires operation at low voltages (around 1 V).
- This difference becomes even more significant for *light doping levels*, where the electron mobility can reach 8000 to 9000 cm^2/Vsec at room temperature. This is approximately 10–20 times higher than silicon. Special devices such as the HEMT (*high electron mobility transistor*) have been developed to exploit this feature. These structures produce some of the fastest logic available, especially at lower temperatures.

- Unfortunately, holes in GaAs do not exhibit equally desirable properties. The hole velocity is approximately 15–20 times lower compared to the GaAs electron. This means that the *complimentary structures are not as desirable* in GaAs as they were in Si.
- Due to very high levels of surface-state charge, structures like *metal-oxide-semiconductor transistors are not possible*. Most GaAs designs, therefore, make use of MESFET (metal-semiconductor field-effect transistor) devices, which are introduced in the next section.
- Pure GaAs is *semi-insulating* with a resistivity between 10^7 and 10^9 Ω·cm at room temperature. This means that devices made of doped GaAs can be isolated from each other by the insertion of undoped material, although additional isolation can be provided by selective ion implantation. This is more area-effective than the field-oxide approach in CMOS. It also has the advantage of reducing the parasitic capacitance.
- Due to a larger band-gap and the semi-insulating substrate, GaAs has the advantage of being more *immune to radiation effects*. It is therefore attractive for space and military applications where it is in direct competition with silicon-on-insulator technologies.
- Finally, but most importantly, GaAs is an extremely brittle and fragile material. For this particular reason, GaAs wafers tend to be no larger than three inches, whereas six-inch and larger silicon wafers are common. This results in a *reduced manufacturing efficiency*. Moreover, getting a reasonable yield has been challenging due to the high defect density in the basic material and the tight device requirements.

The MESFET Device

As mentioned previously, the lack of a MOS-style device has made the MESFET (metal-semiconductor FET) the device of choice in GaAs design. A cross-section of an *n*-MESFET is shown in Figure C.2. It consists of a conductive *n*-type surface channel with a

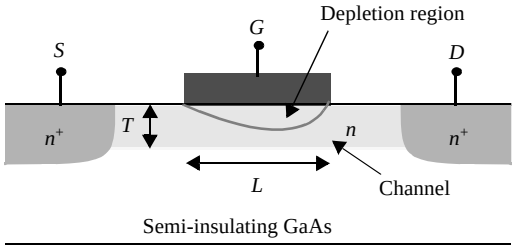


Figure C.2 Cross-section of a GaAs MESFET.

thickness *T*, located between two n^+ ohmic contacts that act as source and drain. Semi-insulating GaAs is used as the substrate material. The device control terminal (the gate) is implemented by depositing a metal (typically Ti/Pd/Au, although Al, W, and Pt alloys work as well) on a section of the channel, so that a *Schottky-barrier diode is created*. A Schottky diode is a metal-semiconductor junction formed by depositing a small metal con-

tact onto a lightly doped *n*-type semiconductor. The resulting diode relies on single-carrier conduction, what results in fast switching times. Appendix D offers a more detailed discussion of this device.

The principles of operation and the basic relationships governing the device are similar to those of the silicon-junction FETs (JFET) and MOSFETs. The MESFET is a unipolar transistor, which means that conduction is dominated by one type of carrier, in this particular case the electron. Its operation is can be understood from the following qualitative analysis:

- Under zero-bias conditions ($V_{GS} = 0$), a depletion region is created under the gate due to the built-in voltage of the metal-semiconductor junction, as shown in Figure C.2. This reduces the number of mobile carriers present in the channel. Typically, the thickness of the depletion layer is smaller than T, which means the channel is still conducting. The nominal MESFET transistor is therefore a *depletion* device.
- Applying a positive voltage to the gate reduces the width of the depletion layer. This increases the conductivity of the channel. However, once the gate-channel voltage is sufficiently high, the Schottky diode becomes forward-biased, and current starts flowing into the gate. As no further increase in conductivity occurs from that point on, this condition is to be avoided in general. The voltage at which forward conduction of the gate occurs depends upon the gate metal and ranges around 0.5–0.7 V.
- When the gate voltage is reduced, the depletion region extends, and the channel conductivity drops owing to the smaller cross-sectional area of the conducting channel. This trend continues until the depletion region extends through the conductive layer (or $W_{depl} > T$) and pinches off the channel. At that point, the transistor is turned off as the channel conductivity drops to 0. The gate-source voltage needed to make this happen is called the *pinch-off voltage* V_P. The pinch-off voltage is analogous to the threshold voltage in a MOS transistor and is a function of the thickness of the channel, the doping level, and the built-in voltage of the Schottky diode. Typical values of V_P for the depletion devices range from –0.7 V to –2.5 V.

As the depletion device is the generic MESFET GaAs transistor, it is tempting to build logic gates using only these devices, as was the case in the earlier days of GaAs digital design. Unfortunately, such a design approach requires the availability of multiple supply voltages—the gate-source voltage has to be negative to turn the device off, while the drain-source voltage has to be positive for conduction.

An enhancement device can be realized by either reducing the channel thickness or by ion implantation, ensuring that channel pinch-off is achieved under zero-bias conditions. The logic swing for an enhancement-based logic gate is limited to the difference between the pinch-off voltage, which normally ranges between 0 and 0.2 V, and the voltage at which the Schottky-barrier diode begins to conduct (around 0.7 V). Under these low swing conditions, small variations of the pinch-off voltage can have a dramatic impact on the circuit's functionality or performance. The realization of complex circuits, therefore, requires an accurate control of the channel thickness over the complete wafer to minimize pinch-off voltage variations.

The device model for the GaAs MESFET is remarkably similar to the MOSFET one. An extra factor is included to incorporate the effects of velocity saturation.

$$I_D = \begin{cases} 0 \text{ for } (V_{GS} < V_P) \\ \beta(V_{GS} - V_P)^2(1 + \lambda V_{DS})\tanh(\alpha V_{DS}) \text{ for } (V_{GS} > V_P) \end{cases} \quad \text{(C.1)}$$

This model, called the *Curtice model* after its inventor [Curtice80], includes both the linear and saturation regions and is an empirical fit using the hyperbolic tangent function. The gate diode is modeled by the traditional diode equation

$$I_D = I_S(e^{V_G/n\phi_T} - 1) \quad \text{(C.2)}$$

A later model, named Raytheon, improved the Curtice model on two fronts: (1) improved I_D versus V_{GS}, and (2) better capacitance models. The parameters for some state-of-the-art GaAs devices are given in Table C.1. For the same process, the threshold voltages for the enhancement and depletion devices can vary between (0.18 V … 0.3 V) and (–0.735 V … –0.92 V), respectively. To obtain the actual values for a particular transistor, the β and I_S values have to be multiplied by the device ratio (W_{eff} / L_{eff}) and the effective gate area ($W_{eff} \times L_{eff}$), respectively. W_{eff} and L_{eff} stand for the effective transistor width and length.

$$\begin{aligned} W_{eff} &= W - \Delta W \\ L_{eff} &= L - \Delta L \end{aligned} \quad \text{(C.3)}$$

For the process presented here, ΔL and ΔW equal 0.4 μm and 0.15 μm, respectively.

Table C.1 Typical transistor parameters for a 1.0 μm GaAs process.

	β (A/V^2)	V_{P0}(V)	λ (1/V)	α (1/V)	I_S (A)	n
Enhancement	250×10^{-6}	0.23	0.2	6.5	0.5×10^{-3}	1.16
Depletion	190×10^{-6}	–0.825	0.0625	3.5	10^{-2}	1.18

Example C.1 GaAs MESFET Current-Voltage Characteristics

The simulated voltage-current characteristics of a (4 μm/1 μm) GaAs MESFET enhancement transistor, implemented in the GaAs process of Table C.1, are plotted in Figure C.3. The most important feature differentiating the device from the MOSFET transistor is the presence of the Schottky diode between gate and channel. From the V_{GS}-I_D curve, we can see that this diode becomes forward-biased once V_{GS} approximately equals 0.75 V. This means that for low values of V_{DS}, the drain current actually becomes negative, as observed in the I_D-V_{DS} curves (encircled). Notice also that the device is velocity-saturated for most of the voltage range of interest.

We can see a close correspondence between the simulated results and the model of Eq. (C.1). For instance, for V_{GS} = 0.5 V and V_{DS} = 2 V, the Curtice model Eq. (C.1) yields the following current value:

$$\begin{aligned} I_D &= \left(\frac{4 - 0.15}{1 - 0.4}\right) \times 250 \times 10^{-6}(0.5 - 0.23)^2(1 + 0.2 \times 2)\tanh(6.5 \times 2) \\ &= 163.7 \text{ μA} \end{aligned} \quad \text{(C.4)}$$

which is close to the simulated value.

The Curtice model is by no means the ultimate in the modeling of GaAs MESFETs. More advanced models include effects such as drain-induced threshold variations, as well as more complex curve-fitting techniques.

The HEMT Device

While the MESFET is used in the majority of the GaAs digital designs, the HEMT (High Electron Mobility Transistor) is the device of choice when extreme performance is required. The cross-section of such a device is shown in Figure C.4. Its operation relies on

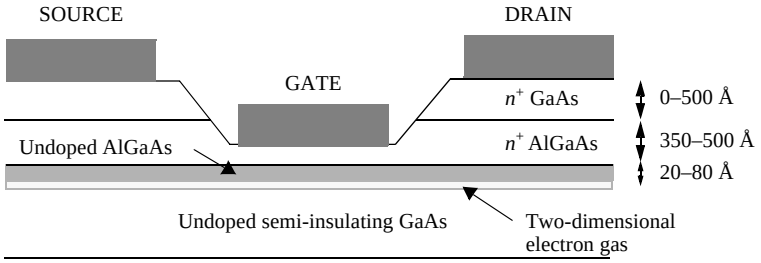
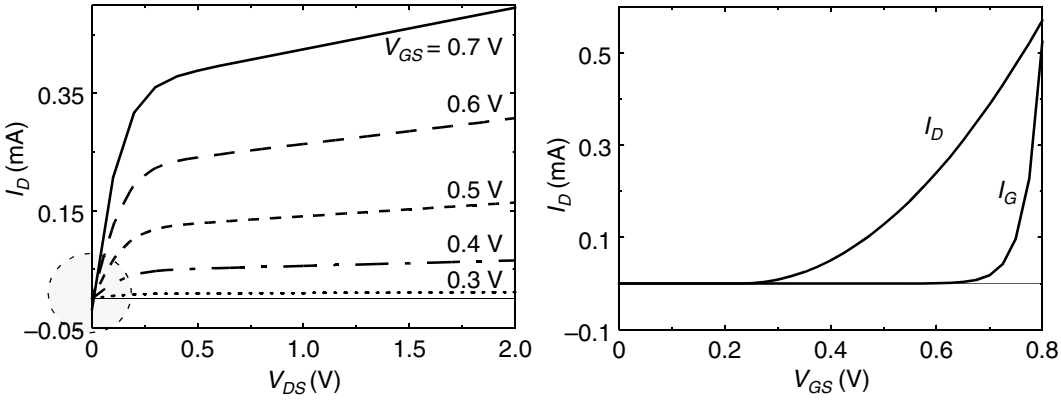


Figure C.4 Cross-section of AlGaAs/GaAs high electron mobility transistor (HEMT) (from [Dingle78]).

the fact that mobility of the carriers is much higher in an undoped region than in a doped material. The HEMT structure separates the donor regions (n^+ AlGaAs) that produce the electrons, but impede high mobilities, from the conducting channel (undoped GaAs) with its very high mobility. AlGaAs is selected as donor material because it has a wider bandgap (1.8 eV) than GaAs (1.4 eV). This causes free electrons from the ionized donors to diffuse to the undoped material due to the electron's inherent affinity to move to the lower bandgap region. Electron mobilities of 8500 cm^2/Vsec can be achieved in HEMT transis-



(a) I_D-V_{DS} characteristic

(b) I_D-V_{GS} characteristic (V_{DS} = 0.5 V). I_G is the current flowing into the gate.

Figure C.3 Current-voltage characteristics of GaAs enhancement transistor (W= 4 μm, L = 1 μm).

tors, compared to the channel mobilities of 4500 cm^2/Vsec in GaAs MESFETs (at 300 K). The situation is even more extreme at lower temperatures (e.g., 77 K, the temperature of liquid nitrogen), where impurity scattering is the dominant mechanism limiting carrier velocity. Mobilities of up to 50,000 cm^2/Vsec have been obtained for HEMT devices operating in this temperature range.

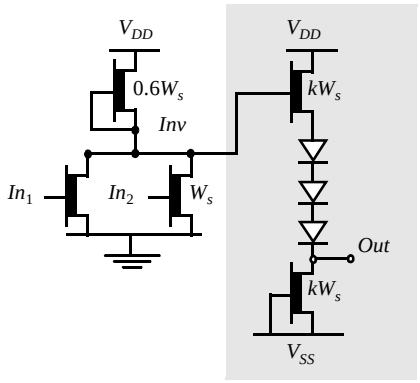
From an operation point of view, the device of Figure C.4 belongs to the class of the MESFETs with the gate Schottky diode formed by the junction of the gate metal and the n^+AlGaAs layer. This diode has the advantage of having a larger turn-on voltage (~ 1V) than its GaAs counterpart, which provides larger noise margins. Depletion and enhancement devices can be constructed. Consequentially, the GaAs MESFET gate structures described below are just as applicable to HEMT devices.

In addition to the MESFET HEMT, other structures have been devised that demonstrate extreme performance, such as the *heterojunction bipolar transistor* (HBT) [Asbec84]. A discussion of these devices would lead us too far astray. It suffices to say that heterojunction devices provide the highest performance at present (barring superconducting gates) and are intensively used in the most demanding applications, such as radio front-ends operating in the high GHz range.

C.2.2 GaAs Digital Circuit Design

Buffered FET Logic

The design of reliable digital circuits in the GaAs MESFET technology has proven to be quite a challenge. A first approach is to use *depletion devices only*. An example of such a gate, implemented in the so-called buffered FET logic (BFL) logic style, is shown in Figure C.5. Two supply voltages, V_{DD} and V_{SS} (4 V and –2.5 V, respectively) are needed.



(a) Input stage (b) Level-shifting output stage

Figure C.5 Two-input NOR gate in buffered FET logic (BFL). The italic numbers indicate the relative transistor sizes. Notice also the symbols used for the depletion MESFET devices.

The first stage implements the logic function, in this case a two-input NOR gate, and is similar to a traditional depletion-load NMOS gate (see Chapter 4). The main difference

is that the pull-down devices are depletion transistors as well, requiring negative input levels to turn them off. The low input level has to be lower than V_P. On the other hand, V_{OH} cannot be higher than $V_{D(on)}$, which is the turn-on voltage of the Schottky diode. The output of the depletion-load inverter is located between *GND* and V_{DD}. A source-follower output stage with level-shifting diodes is inserted to adjust these levels so that all stated requirements are met. This output stage has the additional advantage of making the performance of the gate relatively insensitive to fan-out loading or capacitive loads.

This structure has proven to be relatively insensitive to processing and power-supply variations, which is useful when the processing is not well controlled.

Example C.2 Parameter Variations in BFL

The impact of variations in the pinch-off voltage of the MESFET devices on the dc parameters of a nine-input BFL NOR gate was examined in [Milutinovic90]. Changing the threshold from –1.25 V to –2.0 V causes only a 0.6 V shift in the switching threshold V_M, while V_{OH} and V_{OL} change by at most 0.2 V. A further change in the pinch-off voltage to –2.2 V causes the gate to fail.

The structure also suffers from three major disadvantages:

1. It is based on ratioed logic, which means rise and fall times can be very different.
2. The power consumption is high. The dissipation per gate is typically between 5 and 10 mW, most of which can be attributed to the output stage. This prevents its use in large-scale designs (> 2000 gates).
3. It uses two supply voltages, which is not attractive from a system perspective.

Example C.3 DC Characteristics of the BFL Inverter

A BFL inverter is designed using the depletion devices characterized in Table C.1. All devices have a (*W/L*) ratio of (4 μm/1 μm) with the exception of the load device, which is made 0.6 times smaller. The supply voltages V_{DD} and V_{SS} are set at 3.5 V and –2 V, respectively.

The current through the inverter stage is approximated by the following expression, assuming that both devices are on and that all Schottky diodes are off:

$$\left(\frac{3.85}{0.6}\right)(V_{in} + 0.825)^2(1 + 0.0625V_0)\tanh(3.5V_o)$$

$$= \left(\frac{2.25}{0.6}\right)(0.825)^2(1 + 0.0625(3.5 - V_o))\tanh(3.5(3.5 - V_o))$$

Solving this equation for various values of V_{in} yields the voltage-transfer characteristic of the input stage. Finding this solution is made complex by the presence of the transcendental functions. This can be addressed by using recursive equations solvers. For instance, for V_{in} = 0V, a V_{out} of 0.25 V is found, which is extremely close to the simulated value. The results of a dc analysis are found in Figure C.6 for a fan-out of one identical gate. The simulation plots the output of the inverter as well as the buffer stages. Two issues are worth raising:

1. For input values lower than the threshold of the input transistor, the output of the buffer stage (V_{inv}) is high and equals 3.5 V. Once the input device is turned on, the output

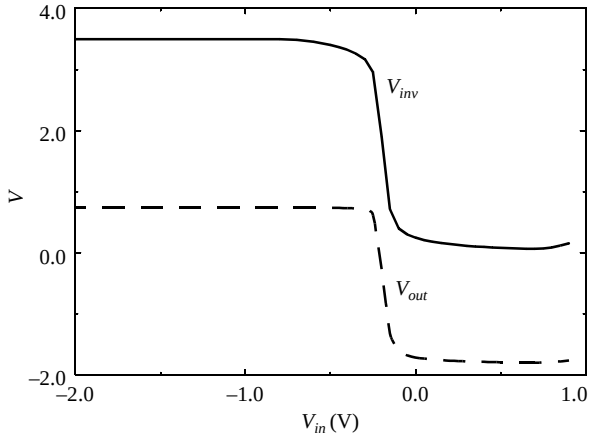


Figure C.6 Voltage-transfer characteristic of BFL inverter (V_{DD} = 3.5 V, V_{SS} = –2 V).

starts to drop until a value of 70 mV is reached for an input of 0.6 V. Raising the input even more turns on the input diode, and the output starts to rise.

2. V_{out} tracks V_{in} fairly accurately. The high value of V_{out} is set by the input diode of the fan-out gate, which turns on around 0.75 V.

The following gate characteristics can be derived from the simulation:

$$V_{OH} = 0.75 \text{ V}, V_{OL} = -1.8 \text{ V}, V_{IH} = -0.06 \text{ V}, V_{IL} = -0.25 \text{ V}, V_M = -0.2 \text{ V}$$
$$NM_H = 0.81 \text{ V}, NM_L = 1.55 \text{ V}.$$

Direct-Coupled FET Logic

One way to avoid the dual supply voltages is to use a combination of depletion and enhancement devices. The latter are used for the implementation of the logic function, while the depletion transistors serve as loads. The resulting structure is, not surprisingly, the depletion-load inverter, which is well known from the early MOS digital design era. In GaAs jargon, such a structure is called a direct-coupled FET logic (DCFL) gate, an example of which is shown in Figure C.7. Some major differences from its MOS counterpart are worth mentioning.

- The value of the high input voltage is limited by the onset of the gate conduction in the pull-down transistor, which ranges between 0.6 and 0.7 V.
- The low level is dangerously close to the threshold voltage of ± 0.1 V. This requires a strict control of the pinch-off voltage.
- Furthermore, the gate inherits all the bad properties of the depletion-load gate, such as asymmetrical transient response and static power consumption.

While achieving propagation delays similar to BFL, the DCFL structure consumes substantially less static and dynamic power. This is illustrated in Figure C.8, which plots

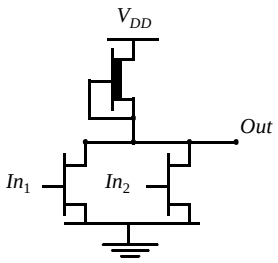


Figure C.7 Two-input NOR gate in direct-coupled FET logic (DCFL).

the propagation delay of DCFL and BFL gates as a function of the power consumption, all designed in a 1 micron technology. An order of magnitude difference in power dissipation is observed for similar performance, if one manages to keep the threshold under control. The BFL gate, on the other hand, has superior fan-out driving capabilities.

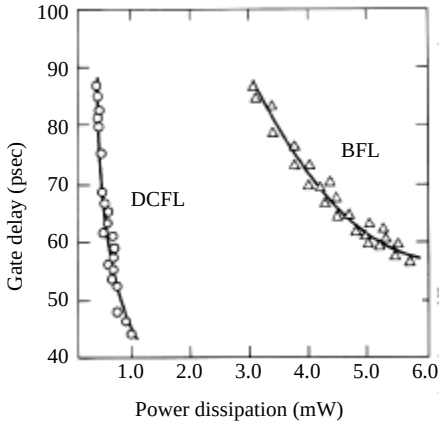


Figure C.8 Comparing the power consumption and gate delay of DCFL and BFL gates (from [Singh86]).

Source-Coupled FET Logic

The concerns about the limitations of FET threshold control in DCFL have prompted the development of another logic family with a wide allowable threshold range. The inspiration for this family, called source-coupled FET logic (SCFL), can be directly traced to the bipolar ECL structure. It consists of a differential pair and two source-follower output buffers with diode level-shifters (Figure C.9). Proper operation of the gate requires only that the input transistors of the differential pair be well matched. As with ECL, the power supply noise is reduced, making it possible to operate with small noise margins. All other considerations raised with respect to ECL gates, such as differential versus single-ended, are valid here as well. While SCFL overcomes the tight threshold control associated with DCFL and is intrinsically faster, its power dissipation is higher than DCFL but less than BFL.

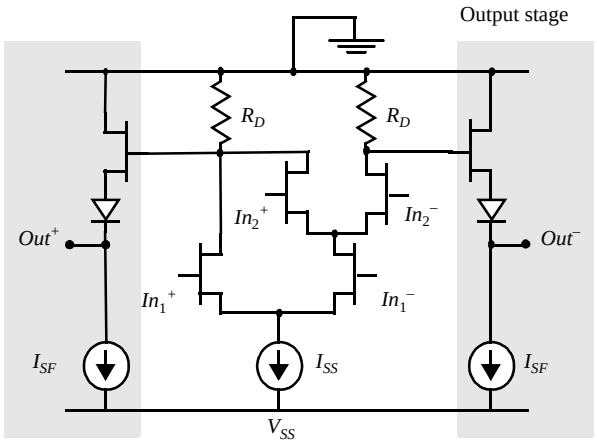


Figure C.9 Two-input NOR gate in differential source-coupled FET logic (SCFL).

Example C.4 MESFET Source-Follower

Consider an inverter in SCFL with $V_{D(on)} = 0.7$ V, $V_{OH} = -1.3$ V, $V_{OL} = -1.7$ V. Using the transistor parameters of Table C.1, determine the value of the I_{SF} such that the voltage drop between the gate and source of the source-follower equals 0.5 V in the midpoint of the voltage transition (assuming that the W_{eff} / L_{eff} of the source-follower devices equals 10).

In the midpoint of the voltage swing, it holds that $V_{out} = -1.5$ V. From the input data, we derive the following data for the source-follower: $V_{DS} = 0.8$ V and $V_{GS} = 0.5$ V. Plugging these numbers into Eq. (C.1) yields a required drain-source current of 0.21 mA. For this current level, the voltage drop over the source-follower is virtually constant over the complete voltage range of interest. Because the transistor operates in the saturation region, a variation of only 9 mV can be observed between the high and the low output levels.

It is left as an exercise for the reader to determine the value of R_D and the sizes of the transistors in the current switch. You may assume that $I_{SS} = I_{SF}$.

GaAs Performance: A Comparison

To put the gates presented here in perspective, Table C.2 presents the measured performance of a number of GaAs logic families (from [Hodges88]). The table presents the delay for a fan-out of 1 (t_{p0}), the sensitivity to fan-out ($\Delta t_p/FO$), and capacitance ($\Delta tp/C_L$) and the power consumption per gate P.

Table C.2 Typical performance of GaAs logic families.

Logic Family	t_{p0} (psec)	$\Delta t_p/FO$ (psec/FO)	t_p/C_L (psec/fF)	P (mW/gate)
BFL (1 μm)	90	20	0.67	10
BFL (0.5 μm)	54	12	0.67	10
DCFL (1 μm)	54	35	1.84	0.25
SCFL	BFL range	low	low	~5
DCFL HEMT (0.5 μm - 77 K)	11	7	0.32	1.3

GaAs Design Space

Digital GaAs excels in the domain of extremely fast, small-scale integration components—frequency dividers, counters, (de) multiplexers—where multi-GHz operation has been achieved. For instance, an 8-bit multiplexer implemented in BFL has been demonstrated to run at 3 Gbits/sec. These circuits can be of interest in very high speed communication systems.

Yield issues, as well as power dissipation limitations rapidly come into play when attempting large-scale integration. To demonstrate what can be achieved, consider first the case of the digital multiplier. The average gate/delay as a function of the power dissipation for a number of multipliers is plotted in Figure C.10. Actual gate propagation delays of 60 psec and 170 psec have been achieved for the HEMT and MESFET technologies, respectively. This translates into multiplication delays of 4 nsec for a 16×16 multiplier (at room temperature) with the power dissipation in the multiple (1–6) watt range.

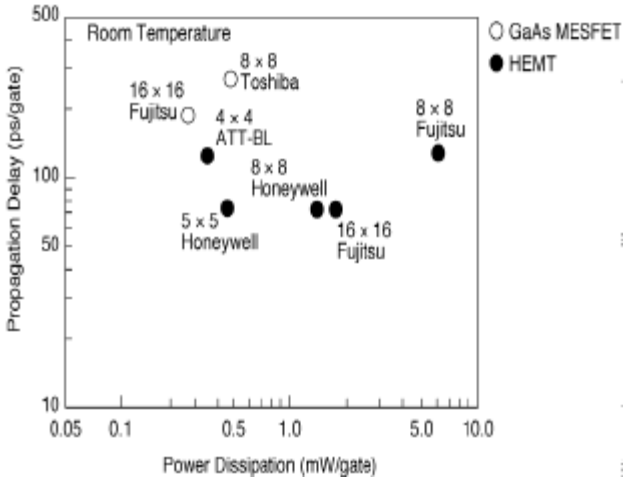


Figure C.10 Comparison of GaAs MESFET and HEMT multiplier propagation delays as a function of power dissipation (from [Abe89]).

Other larger-scale modules have been implemented, such as SRAM memories (4.1 nsec access time for a 16K memory) and gate arrays (up 3000 gates operating at 700 MHz). Multiple attempts have been made to use GaAs technology for the implementation of supercomputer and mainframe processors as well as microprocessors, but these efforts have largely proven

unsuccessful. Although working prototypes have been demonstrated, manufacturing and economic constraints have prevented these components from reaching the market.

C.3 Low-Temperature Digital Circuits *

An alternative approach to higher performance is to operate the devices at lower temperatures. The carrier mobility in most devices increases dramatically when the temperature is reduced. Besides the increased mobility, cooling further enhances the performance and reliability of digital integrated circuits, improving the subthreshold slope, the junction leakage current and capacitance, and the interconnection resistance. Some non-scalable parameters such as the thermal voltage, are also reduced when the temperature is lowered.

While this sounds attractive, cooling comes at substantial cost. High-quality coolers are expensive, bulky, and consume extra power. The most popular cooling media in use are the inert gases, nitrogen and helium, which have boiling temperatures of 77 K and 4.2 K, respectively. While liquid nitrogen is inexpensive, and cooling costs are moderate, operating at liquid helium temperatures allows for superconductive operation.

In this section, we briefly discuss the operation of silicon at lower temperatures as well as the nature and potential of superconducting digital circuitry.

C.3.1 Low-Temperature Silicon Digital Circuits

Cooling results in an increase of both saturation velocity and carrier mobility for MOS devices. Simultaneously, the junction capacitance is reduced due to the *freeze-out* effect, which means that the dopant atoms hold on to their extra electrons and holes at low temperatures. This results in wider depletion regions, and consequently smaller capacitances. All the above helps to reduce the intrinsic delay of the MOS gate. The impact of cooling on some of the MOS device parameters is shown in Table C.3.

Table C.3 Measured device parameters as a function of temperature. The numbers quoted are for an NMOS transistor, with the corresponding values for a PMOS device between brackets (from [Ghoshal93a]).

Parameter	300 K	77 K	4 K
V_T (V) ($@I_D$ = 0.1 μA)	0.12 (0.08)	0.3 (–0.18)	0.35 (–0.29)
μ_{fe}(cm^2/V·sec)	490 (220)	2300 (1000)	4400 (3500)
I_{Dsat} (mA/mm)	31 (16)	57 (29)	61 (30)
Subthreshold slope (mV/decade)	74 (81)	21 (28)	5.7 (9.4)

Combining the increased current drive with the reduced capacitance results in a performance increase by a factor of two-to-three for liquid nitrogen operation, and even more when operating at 4 K.

At the same time, *leakage currents* are substantially reduced, because the leakage current of a junction (I_S) is a strong function of the temperature ($\sim e^{qV_j/kT}$). The reduced sub-threshold slope of the device further reduces leakage and makes it possible to operate at lower threshold voltages. At 4 K, a dynamic gate behaves as a static structure, and refresh is no longer necessary.

Finally, reducing the temperature also decreases the interconnect *resistivity*, because the carriers have less thermal energy, and the scattering rate is subsequentially reduced. At liquid nitrogen temperatures, the resistance of aluminum wires improves by a factor five to six [Bakoglu90].

Besides the cost and difficulty of the providing high-quality cooling environments, operation at a reduced temperature has some disadvantages.

- The mentioned carrier freeze-out increases the resistance of the source and drain regions, since fewer mobile carriers are available. It also causes the threshold voltage to increase, as Table C.3 shows. Due to the freeze-out, less of the ion-implanted impurities in the channel are being ionized.
- Threshold voltages in cooled MOS devices tend to drift with time due to hot-electron trapping effects, as carriers injected into the gate are more likely to be trapped. This effect can be remedied by operating at lower voltages.
- The current gain of *bipolar devices* degrades at lower temperatures due to bandgap narrowing and reduced emitter-base injection. While this helps to suppress parasitic effects such as latchup and subthreshold conduction in MOS transistors, it precludes the use of bipolar gates at temperatures lower than 77 K.

Cooling has been frequently used in the design of high-performance mainframe and supercomputing systems. For instance, the ETA supercomputer (1987) uses liquid nitrogen cooling to reduce its cycle time from 14 nsec at room temperature to 7 nsec. Another emerging approach is to combine MOS silicon structures with superconducting logic. This exploits the extreme performance of the superconducting circuitry with the high density of MOS. It is worth noting that dynamic circuits exhibit a better behavior at liquid helium temperatures, as leakage is eliminated and noise signals are reduced [Ghoshal93b].

C.3.2 Superconducting Logic Circuits

The use of superconductivity in digital circuits dates back to the 1950s. The development of the Josephson junction at IBM [Josephson62] spurred the quest for a superconducting computer. While this effort faltered in the early 1980s, the 1990s witnessed a renewed interest in this technology for two reasons: (1) the discovery of high-temperature, superconducting alloys, and (2) the introduction of niobium junctions, which provide increased reliability and performance compared to the earlier lead-alloy-based junctions. Before discussing the Josephson junction, which is the prime switching element in superconducting logic, we first describe superconductivity.

Superconductivity

A number of materials have the property to *conduct current without resistance* when cooled below a critical temperature T_c. Until recently, most of the known superconducting materials exhibited this desirable property only when cooled close to absolute zero. In the late 1980s, a new class of superconducting ceramic materials was discovered with critical temperatures around and above 100 K. This discovery is important, because it substantially reduces the cooling cost, using liquid nitrogen as a coolant. New composites with ever higher critical temperatures are still being discovered, raising hopes for the availability of room-temperature superconductivity in the near future. One warning with respect to those materials should be heeded: the onset of superconductivity is not only a function of the temperature, but also of the density of the current flowing through the material (J) and the magnetic field present (Φ).

$$T_c = f(J, \Phi) \tag{C.5}$$

Raising either the current density or the magnetic field above a critical value causes the material to revert to the resistive state. For instance, the compound material yttrium-barium-copper-oxide (or YBCO) has a nominal critical temperature of 95 K, which is substantially above the 77 K of liquid nitrogen. Unfortunately, the maximum current density allowed at 77 K equals 4 $\mu A/\mu^2$, which is too low to be useful in digital circuit design.

The potential impact of superconductivity on circuit design is quite large. It enables the transmission of signals over long wires without any resistive loss. This decreases the propagation delay while lowering the power dissipation. Currents can be stored in inductive loops for an almost infinite time, providing for a simple memory structure. In contrast to most digital circuits that can be modeled as *RC*-networks, the first-order model for a superconducting component is closer to an *LC*-network.

The most obvious application of superconductivity in the digital arena is to use traditional devices such as MOS transistors, interconnected by superconducting wires. While this approach helps to address some of the interconnect issues raised in Chapter 8, its impact on overall circuit performance is limited, affecting only the delay of the *RC*-dominated wires. A potential application is the distribution of clocks with minimal skew.

More impressive performance benefits are obtained when employing superconducting switching devices as well. Using this approach, switching delays in the range of picoseconds can be obtained, which is almost an order of magnitude faster than what can be obtained with semiconductor devices. The most popular of these devices is the Josephson junction.

The Josephson Junction

The Josephson junction (abbreviated JJ) was discovered in the early 1960s at the IBM Watson center [Josephson62]. It consists of two layers of superconducting material separated by a very thin insulator (between 1 and 5 nm), as shown in Figure C.11. The material of choice in current superconducting design is niobium, which has a critical temperature of 9 K. The niobium process has the advantage of being substantially more reliable than the lead-alloy processes used in the earlier JJ implementations.

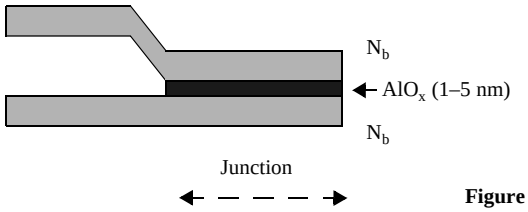
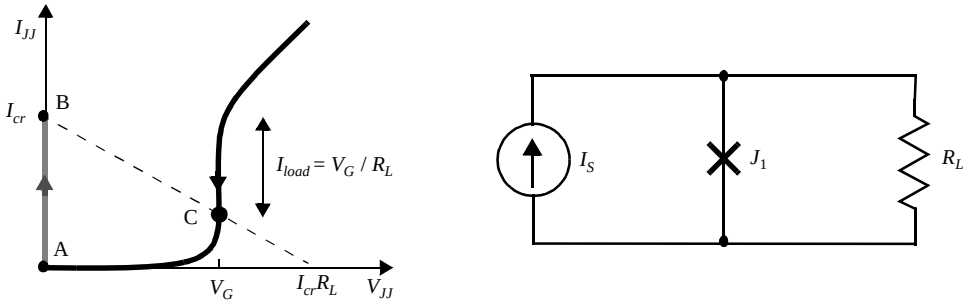


Figure C.11 Nb-AlO_x-Nb Josephson junction.

The Josephson junction is a tunneling device. In the superconductive mode, electrons tunnel from one electrode to the other without voltage loss. The oxide barrier acts as a superconductor. Raising the current level (or adjusting the magnetic field) causes the device to revert to the resistive state, which results in a fixed voltage drop over the junction. For the Nb/AlO_x/Nb junction, the voltage drop over the junction V_G equals 2.8 mV (!).[1]

Consider a JJ junction connected to a shunt resistor R_L and a current source I_S, as shown in Figure C.12b. The behavior of the circuit can be understood by combining the *I-V* characteristic of the junction, represented as a cross in the schematic, with the load-line of the resistor (Figure C.12a). Assume that the junction is initially in the superconducting state. The voltage over the junction is zero, independent of the current level (interval A-B in Figure C.12a). Raising the current keeps the junction in the superconducting state as long as it does not exceed a critical level (I_{cr}). Larger currents (point B) cause the junction to switch to the voltage state represented by the black curve. The voltage over the junction is constant for most of the current range of interest and equal to the energy-gap voltage V_G. A linear resistive-like behavior is observed for higher current levels. The operation point C is determined by the cross-section between the *I-V* characteristics of the junction and the resistor (= I_S - V_{JJ}/R_L). Most of the current is transferred to the load resistor. The critical current I_{cr}, where the switching occurs, is a function of the junction area as well as the applied magnetic field.



(a) *I-V* characteristic of junction (b) Test circuit

Figure C.12 *I-V* characteristic of JJ junction when shunted with load resistor.

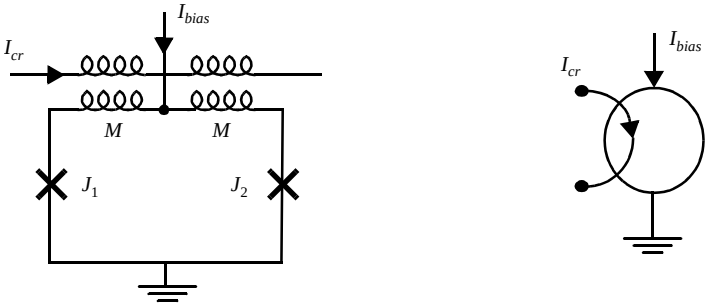
[1] The difference between the superconducting and resistive operation modes of the junction is that in the former, the electrons tunnel through the junction in pairs. For a more detailed description of the underlying concepts, please refer to [VanDuzer89].

As is apparent in Figure C.12a, the Josephson junction displays a hysteresis-like behavior. The junction remains in the voltage stage, even when the current level is dropped below I_{cr}. For the junction to revert to the superconductive state, it is necessary to reduce the current level to zero, as illustrated by the arrow on the curve.

From the above discussion, it becomes clear that the junction can be modeled as a two-terminal device with two operation modes: the superconducting, zero-voltage and the resistive, fixed-voltage state. In a typical operation, the junction is biased with a current I_{bias}, slightly smaller than the critical current I_{cr}. If a switching action is required, the current is slightly raised, causing the junction to revert to the resistive state. Another approach is to apply a magnetic field so that the critical current I_{cr} is lowered below I_{bias}, which has a similar effect (Eq. (C.5)). Lowering the biasing current to zero resets the device to the superconducting state, after which the next operation cycle can commence.

The Josephson junction has the disadvantage of being a two-terminal device. This property makes it less favorable for digital operations, as no isolation exists between inputs and outputs. A control terminal can be added by overlaying an insulated thin (superconductive) wire on top of the junction. Suppose now that the junction is biased with a bias current somewhat below I_{cr}. Routing a current through the control wire causes a magnetic field to pass through the plane of the junction, what reduces the critical current. When the critical current drops below the bias current, the junction becomes resistive. The resulting structure has perfectly isolated input and output terminals.

In general, it is rare to use a single junction in a digital circuit. It is more advantageous to use two or more junctions connected in a superconducting loop or an assembly of loops. Such a circuit is called an *interferometer* or *superconducting quantum interference device* (SQUID). An example of a two-junction SQUID is shown in Figure C.13. A magnetically-coupled control terminal has been added. The magnetic coupling is captured by the mutual inductance M. The I-V characteristic of the SQUID structure is similar to the single junction, but tends to offer larger noise margins.[2]



(a) Schematic diagram (b) SQUID schematic symbol

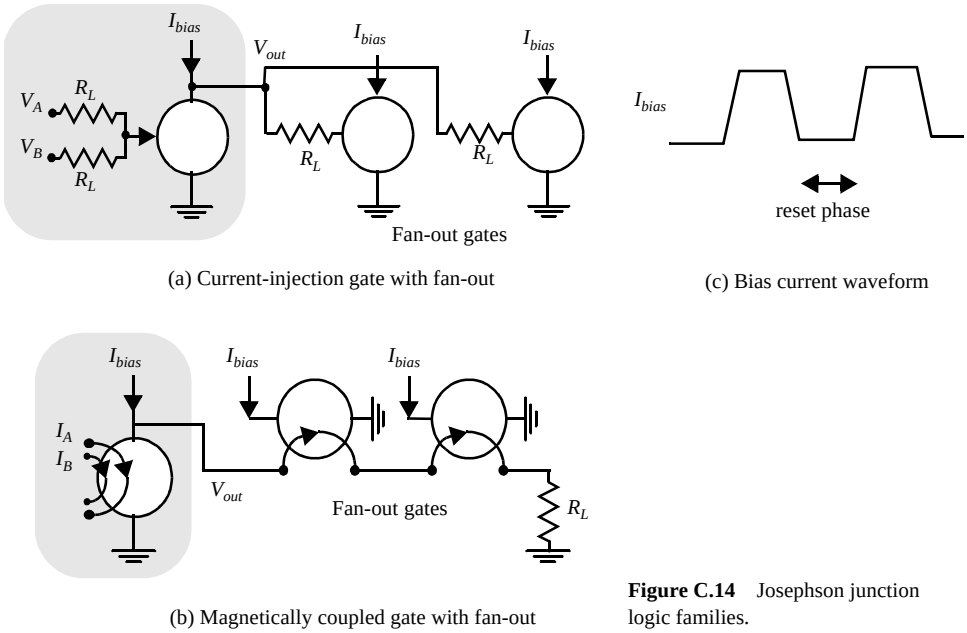
Figure C.13 SQUID with magnetically-coupled control wire.

[2] The actual characteristics of the SQUID are somewhat more complex. For a full discussion of its operation (which is beyond the scope of this text), please refer to [VanDuzer89].

The main attraction of the Josephson junction is its extremely fast switching time. Gate delays in the range of picoseconds have been recorded, which is substantially below what can be achieved in semiconductor technologies, and opens the door for multi-GHz digital circuits. The switching speed is mostly limited by parasitic circuit effects, not by intrinsic constraints. One word of caution: while switching from the superconductive to the resistive state proceeds with incredible speed, the reverse operation (the *resetting* of the junction) is comparatively slow and can take up to 20 psec. The reset phase can be compared to the precharging operation in dynamic MOS circuits. As in the dynamic approach, the impact of the "dead time" on the overall performance can be minimized by adopting the correct system architecture. For instance, it is typical for JJ circuits to operate in a pipelined mode with multiple clocks, where one stage is evaluating while the others are being reset.

Superconducting Digital Circuits

On the basis of the type of control mechanism employed, we can divide Josephson digital circuits into two classes. In the first class, switching between the two states is accomplished by current overdrive or *current injection*, while the second class uses *magnetic coupling* [Hasuo89]. The concepts behind both approaches are illustrated in Figure C.14, where simplified implementations of a two-input OR gate are shown.



(a) Current-injection gate with fan-out

(c) Bias current waveform

(b) Magnetically coupled gate with fan-out

Figure C.14 Josephson junction logic families.

Consider first the current-injection approach (Figure C.14a). The SQUIDs are powered by a pulsed current source, which delivers a current I_{bias}, smaller than I_{cr}. If none of the inputs is high, the junctions in the SQUID stay in the superconducting mode, and V_{out} = 0 V. If either input *A* or *B* is high, an extra current flows into the loop through the resistors R_L. The combination of the bias and the injected currents exceeds the critical current and causes the junctions in the loop to become resistive. The output of the gate moves

from 0 V in the superconducting state to the gap voltage of 2.8 mV. The bias current is diverted from the loop into the connecting fan-out gates, assuming that the on-resistance of the junctions is higher than R_L. Since the output current flows into the SQUID loop of the connecting gates (which is equivalent to stating that the input-impedance of the gate is small), fan-out gates must be connected in parallel.

The magnetically coupled approach (Figure C.14b) relies on a similar idea. If both inputs are low, the SQUID operates in the superconducting mode (V_{out} = 0 V). Applying an input current to one (or both) of the inputs generates a magnetic field that reduces the critical current below the applied bias current. The SQUID switches to the resistive state, and the output switches to high (V_{out} = 2.8 mV). As the input of the gate is physically isolated from the output due to the magnetic coupling, the output signal can be serially connected to multiple cascaded gates.

To initiate the next logic operation, the bias current is lowered to zero (Figure C.14c), and the junctions are reset to the superconducting state.

While these two circuits give an impression of how a Josephson junction logic family can be constructed, the picture is by no means complete. Multiple variants of those logical families have been devised over the years, each of them with varying fan-out, noise-margin and switching-speed properties [Hasuo89]. In fact, a third class of logic styles has emerged called the *hybrid* style. Logic circuits of this class combine current injection and magnetic coupling to achieve better noise margins and faster switching speed. A member of the hybrid gate class is the popular MVTL gate (*modified variable threshold logic*), which is the logic style of choice in most of the larger-scale superconducting designs (see [Kotani90]), and is pictured in Figure C.15. Assume that all junctions are initially in the

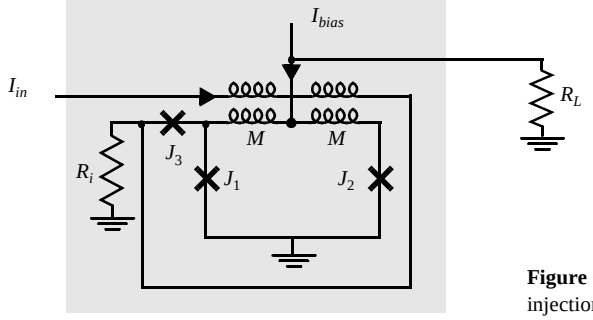


Figure C.15 MVTL gate, combining current injection and magnetic coupling.

superconducting mode and that an input current I_{in} is applied, which could be the OR-ing of two input currents. This current is coupled magnetically to the SQUID loop consisting of junctions J_1 and J_2. At the same time, I_{in} is also injected into the loop through junction J_3. The combination of both current injection and magnetic coupling accelerates the switching of the junctions J_1 and J_2 to the resistive state. If R_i is chosen to be smaller than the load resistance R_L, the bias current is diverted towards R_i instead of the fan-out gate. This causes J_3 to change state and to become resistive, which routes the input current I_{in} into R_i and deflects the bias current to the fan-out gate. The purpose of J_3 is to provide isolation between input and output, a desirable property for digital gates that is typically not present in the current-injection logic families. The hybrid nature of the structure that combines

injection and coupling results in extra-fast operation speeds. In fact, propagation delays of 1.5 psec (!) have been measured for a two-input MVTL OR-gate with a single fan-out.

Example C.5 An MVTL Gate

The layout of an MVTL two-input OR gate is shown in Figure C.16. The input voltages In_1 and In_2 are converted into a current with the aid of the input resistors R_{in1} and R_{in2}. The wire carrying this current is routed on top of the SQUID loop and provides the required magnetic coupling. The bias current is delivered through the resistor R_{bias}, connected to the pulsed supply voltage V_{bias}. The resistor R_D is added to dampen parasitic oscillations in the superconducting LC loop. The gate is implemented in a $Nb/AlO_x/Nb$ technology with a $3\,\mu m \times 3\,\mu m$ minimum junction area.

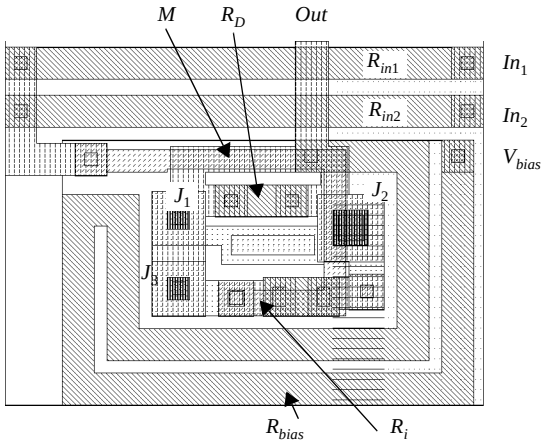


Figure C.16 Layout of a two-input MVTL NOR gate (from [Mehra94]).

The simulated transient response of the gate is plotted in Figure C.17. The observed gate delay approximately equals 20 psec. The small oscillations on the output signal are due to inductive effects. The hysteresis effect of the Josephson junction is apparent. It is necessary to lower the bias current to 0 to reset the output signal.

Even though the gates shown above seem simple, Josephson junction digital design is far from trivial for a number of reasons.

- The gates, in general, are *noninverting*. Implementing an inverter requires a complex clocking scheme. This deficiency can be addressed by using differential logic, and by providing both signal polarities simultaneously, as is customary in the CPL and ECL logic styles discussed earlier.
- The circuits are powered by an *ac-power supply* (or clock). Distributing such a clock at high speeds is complicated. Be aware that a minimum dead time is necessary to ensure resetting of the junctions in between logic operations. To address this issue, complex clocking schemes with up to three clocks are commonly used.
- *Interfacing with the external world* is complicated. The internal signals in a Josephson junction design have a logic swing of only 2.8 mV, while the external world typically requires much larger swings. The conversion process introduces additional delay that hampers the overall performance. Additionally, every connection to the

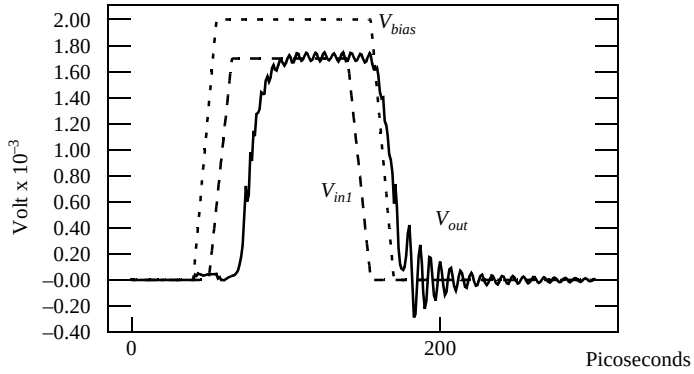


Figure C.17 Transient response of a two-input MVTL NOR gate (V_{in2} = 0). The bias voltage is scaled to fit on the same scale as the input and output signals. Notice how lowering V_{in1} does not cause V_{out} to revert to the superconductive state. This is only accomplished by resetting the bias current.

outside world has to pass through the cooling dewar and introduces heat leaks. The number of connections should therefore be kept to an absolute minimum.

- In general, design at this extreme performance level is exceedingly difficult, since we must address an array of second-order parasitic effects. Signals start to behave as electromagnetic waves, and inductive effects become significant (as discussed in Chapter 8). To keep the delays associated with those parasitics from becoming dominant, a careful sizing of the load resistors is necessary.

Example C.6 A Josephson Signal Processor

Notwithstanding these difficulties, a number of high-density, high-performance circuits have been realized in the Josephson technology. One of the most complex implementations up to the date of writing is a 1 GOPS Digital Signal Processor [Kotani90]. The circuit consists of 6,300 MVTL gates and counts 23,000 Josephson Junctions. The average delay per gate equals only 5.3 psec/gate. An 8×8 multiplication takes a mere 240 psec! The total power consumption of the circuitry, when clocked at 1 GHz, totals 12 mW. This very low dissipation can be attributed to the small logic swing of 2.8 mV. Unfortunately, this benefit is dwarfed by the large amount of power dissipated by the cooling dewar.

C.4 Summary

The following concepts were introduced in this chapter:

- GaAs is a semiconductor material that has the potential to outperform silicon by a factor of 2 (or even higher when heterojunction devices are employed). Achieving this performance boost is complicated by the limited set of device options. Most GaAs designs at present use a MESFET device as the main building block. The main challenge in the design of a high-performance MESFET device is to deal simultaneously with low supply voltages, small logic swings, and variations in the device parameters. A number of logic families have been devised that address these

issues. The most popular ones are BFL, DFL, and SCFL. GaAs designs are attractive for the implementation of small building blocks with very high performance, such as those needed in networking and communication systems.

- Heterojunction devices are gaining rapid recognition as one of the promising techniques for future very high performance design. They exploit the high carrier velocity obtained at low doping levels in GaAs and in other compound semiconductors such as silicon-germanium (SiGe).
- Reducing the ambient operating temperature of a digital circuit results in a significant performance improvement. Cooling a silicon MOS design to the liquid nitrogen range boosts the performance by a factor 2 to 3.
- The fastest digital devices at present use the superconducting technology and achieve switching speeds in the picosecond range. The fundamental building block for most of these designs is the Josephson junction, a current/flux-controlled device with a hysteresis-like behavior. The high performance does not come for free. Providing the necessary cooling medium requires an expensive, bulky dewar. Design at these high speeds is also anything but easy. The main application domain of these devices has therefore been in areas where this extreme performance is essential, such as instrumentation.
- A number of exciting developments, such as the emergence of the high-temperature superconductors, hybrid silicon-superconductor, and other new devices, such as flux quantum transistors, might change this picture in the coming decades.

This addendum concludes with a philosophical consideration. The chapter demonstrates that achieving extreme switching speeds comes at a substantial cost in design effort. Traditional design methodologies and design automation techniques become useless. Interconnections become a significant part of the circuit schematic at these high frequencies and introduce noise and delay. The design of a reliable high-performance circuit typically turns into a lengthy analysis and optimization process. It is furthermore not obvious that scaling technologies into the deep submicron regions will result in sustained performance improvements. Power considerations, for instance, might provide an upper limit on the switching frequencies that are attainable.

Before opting for one of the higher performing, but less designer-friendly and expensive design technologies, we should consider if the performance gain cannot be obtained by other means, for instance by using *concurrent processing*. Too often the clock speed is used as the dominant performance metric. Frequently, the same system performance can be obtained by running multiple slower elements in parallel. This might come at some expense in area but with greatly reduced design effort. This tendency is becoming prevalent in the high-performance computer arena, where supermainframe computers with their extremely high switching speeds are gradually losing out against parallel implementations.

C.5 To Probe Further

A number of specialized textbooks have recently been published on GaAs digital design, a number of which are listed below. Excellent overviews of the state-of-the-art techniques can be found in [Long90]. Once again, the *IEEE Journal of Solid-State Circuits* and the ISSCC conference proceedings are the common source to consult regarding the latest developments in each of these technologies.

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C.6 Exercises and Design Problems

For all problems, use the device parameters provided in Chapter 2 (as well as the book cover), unless otherwise mentioned.

1. [E, None] List the main benefits of using GaAs for digital design. What are the main drawbacks of GaAs circuits?

2. [E, HSPICE] Draw the VTC of the GaAs inverter circuit of Figure C.18. Sweep the input signal between 0 and 0.7 V. Assume (a) a depletion and (b) an enhancement device. Compare the manual results with the output of HSPICE. Use the following models for the MESFET transistors.

```
.model enh njf
+ vto=0.23 beta=250u lambda=0.2 alpha=6.5 ucrit=0 gamds=0 ldel=-0.4u wdel=-0.15u
+ rsh=210 n=1.16 is=0.5m level=3 sat=0 acm=1 capop=1 gcap = 1.2 m crat = 0.666

.model dp njf
+ vto=-0.825 beta=190u lambda=0.065 alpha=3.5 ucrit=0 gamds=0 ldel=-0.4u wdel=-0.15u
+ rsh=210 n=1.18 is=10m level=3 sat=0 acm=1 capop=1 gcap = 1.2 m crat = 0.666
```

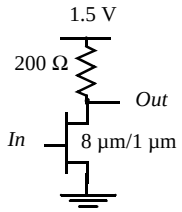

Figure C.18 GaAs inverter.

3. [M, HSPICE] Determine the propagation delay of the buffered FET NOR of Example C.3 as a function of the load capacitance (using HSPICE). Use the models given in Problem 2. For the Schottky barrier diode, use a MESFET with the drain shorted to the source. Discuss the obtained results.

4. [C, HSPICE]

a. Sketch the schematic of a two-input buffered-FET NAND gate. Include the level-shifting output stage(s). Explain the obtained results.

b. Simulate the VTC of the obtained gate (for both inputs).

c. What are the power consumption and propagation delay of the circuit of part (b).

5. [E, None] Using the parameters of Table C.3, determine the speed-up obtained when cooling a CMOS inverter from 300 K to 4 K.

6. [M, None,] Consider the Josephson junction circuit shown in Figure C.19. Assume that $I_{bias} < I_{c1} < I_{c2}$.

a. Determine the logic function of the circuit. Describe its basic operation.

b. Explain why this circuit exhibits input-output isolation. In doing so, assume that a current I_x is injected into the gate from the output.

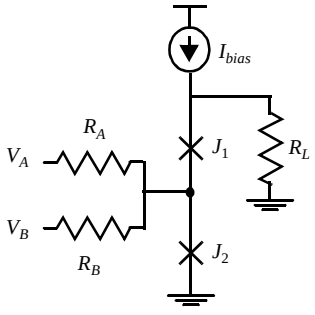

Figure C.19 Josephson junction circuit.

7. [C, None] Discuss the operation of the circuit of Figure C.20. What is its function? What are the output levels?

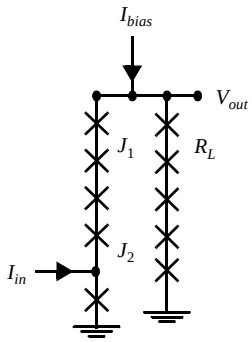

Figure C.20 Josephson junction circuit.