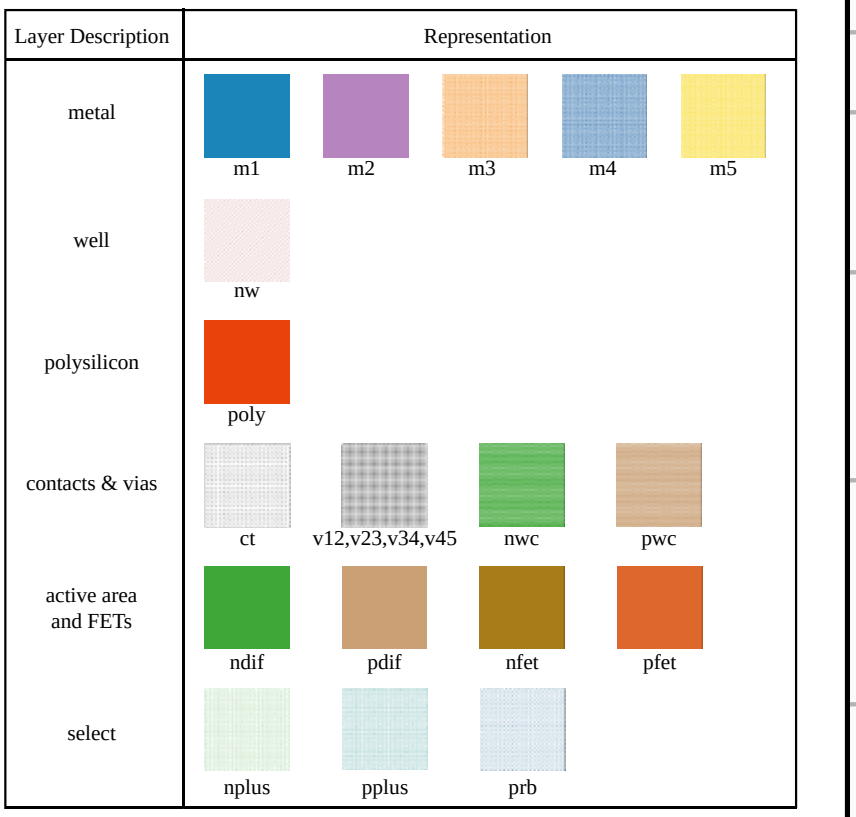
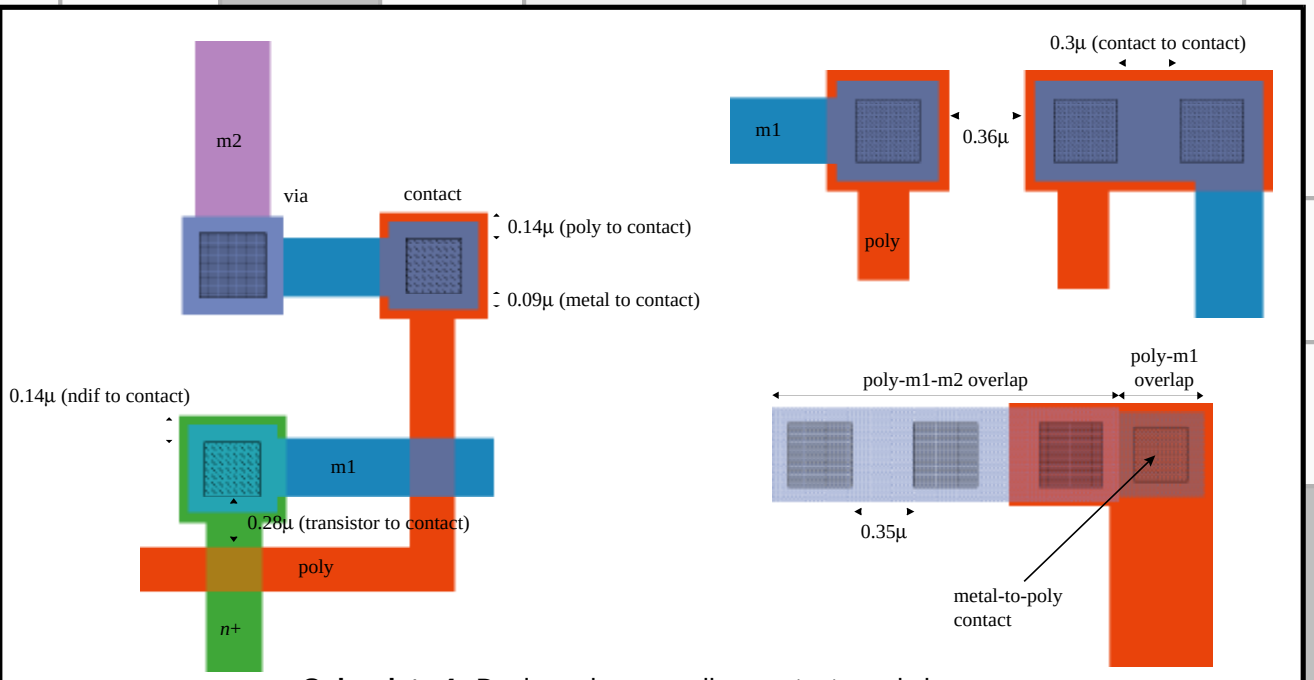
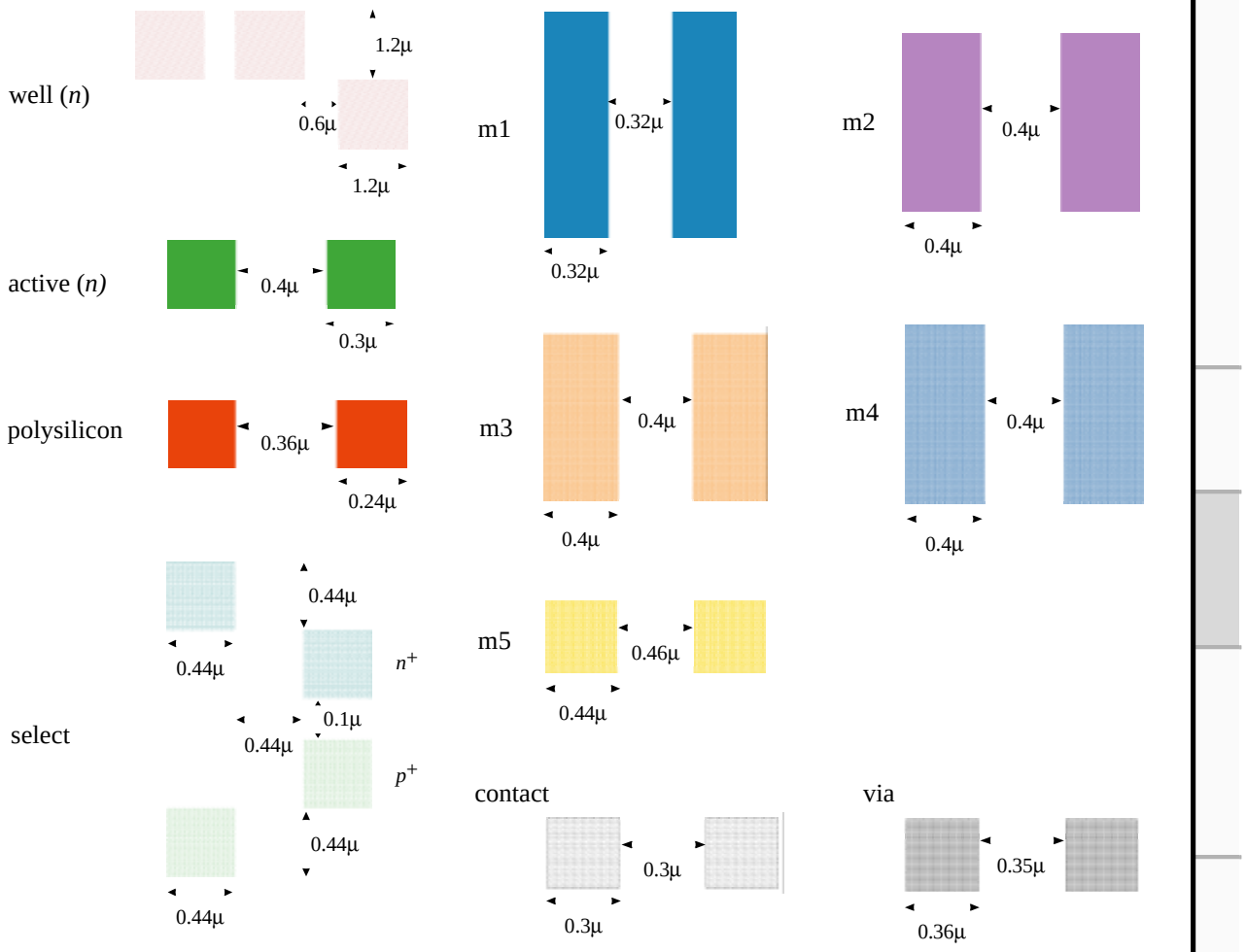


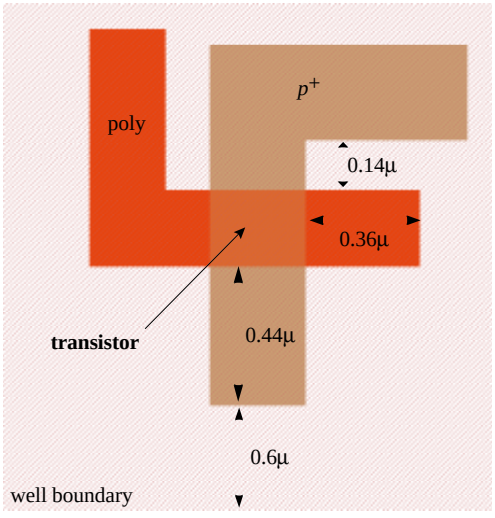
Colorplate 1. CMOS layers and representations (for vanilla 0.25 µm CMOS process)



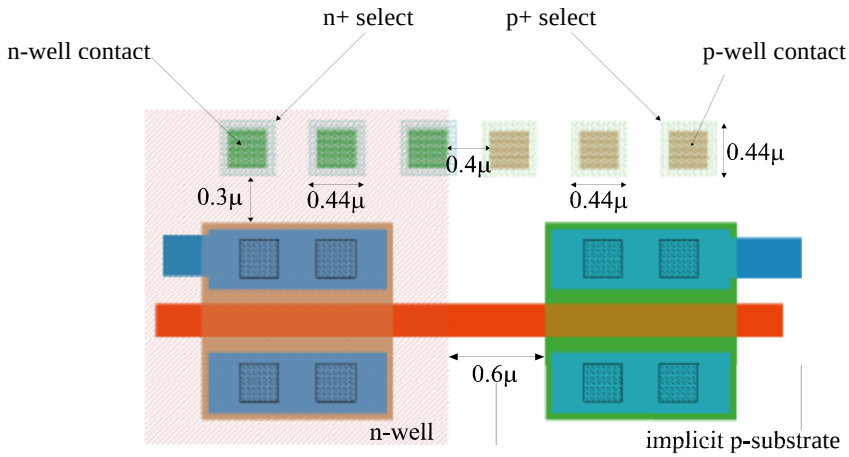
Colorplate 4. Design rules regarding contacts and vias. Overlapping layers are marked by merged colors.



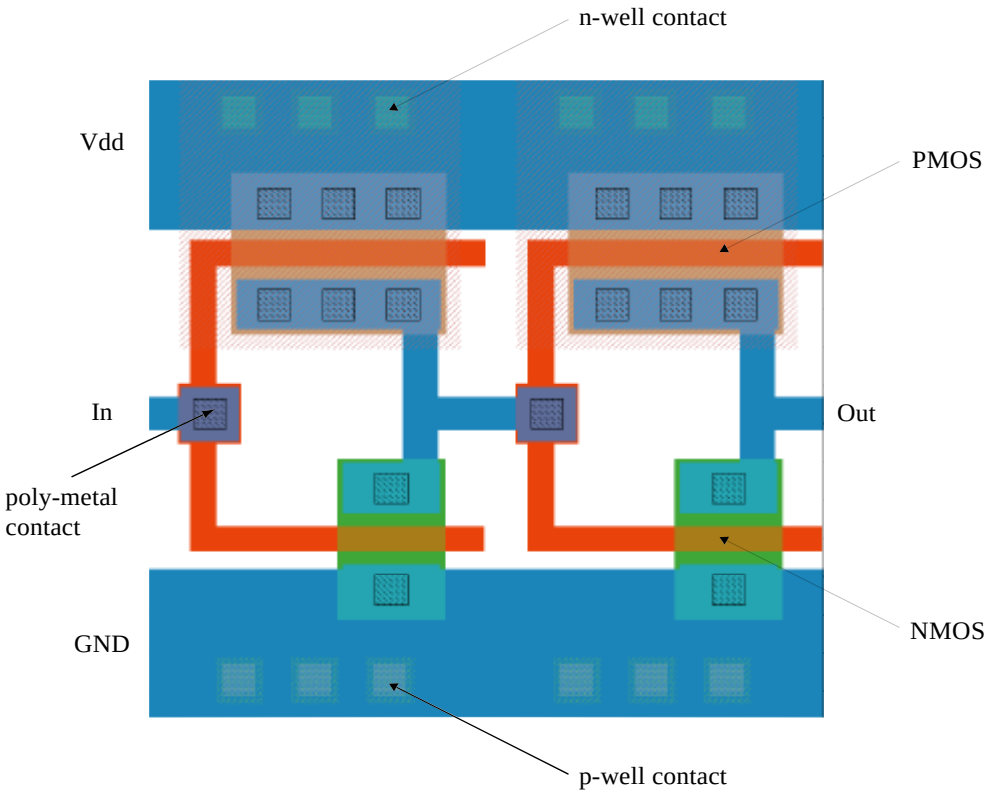
Colorplate 2. Intra-layer layout design rules, expressed as minimum dimensions and spacings.



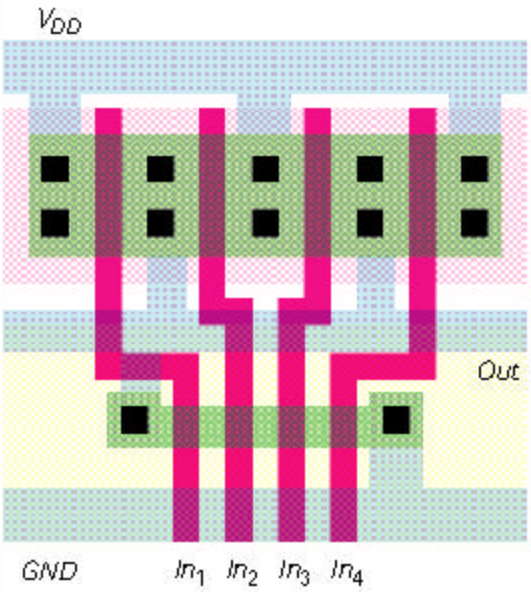
Colorplate 3. Design rules concerning transistor layout. The device shown is a PMOS transistor.



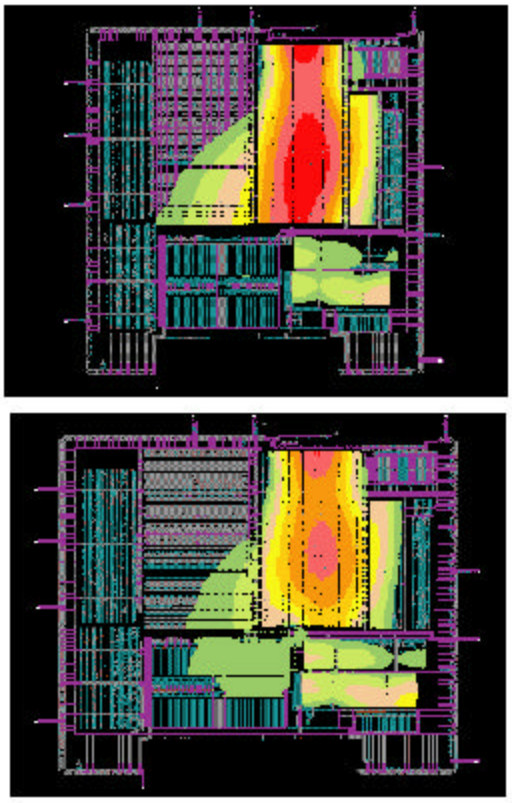
Colorplate 5. Design rules regarding well contacts and select layers.



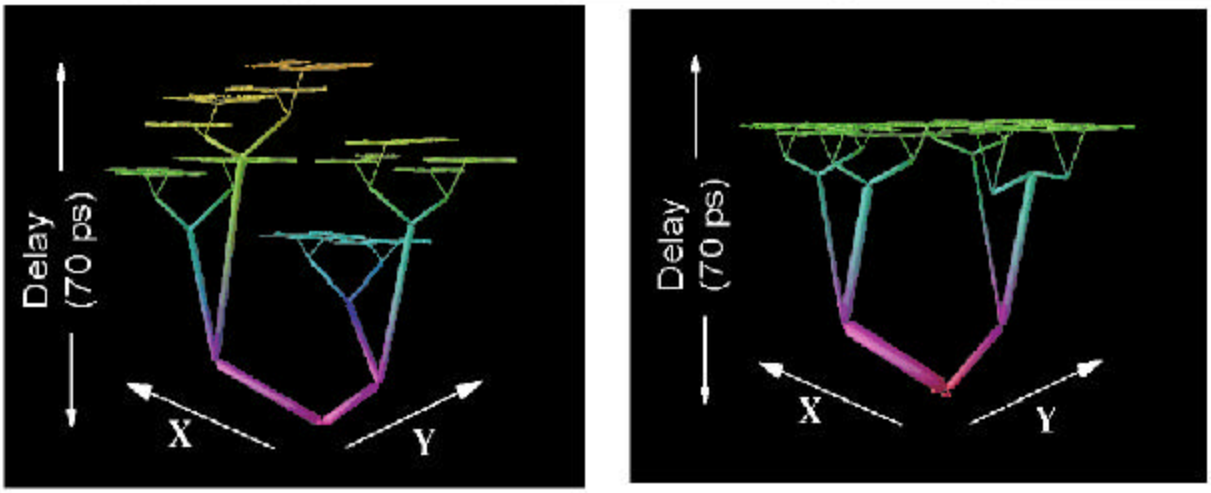
Colorplate 6. Layout of inverter in 0.25 µm CMOS technology.



Colorplate 7. Four-input CMOS NAND.



Colorplate 8. Simulated IR voltage drop in power-distribution network.



Colorplate 9. Visualizations of clock delay in a tree network driving different loads.